REMARKS/ARGUMENTS

Claims 1, 2, 9, 10, 17, 18 and 25 are pending in the present application. Claims 1, 9, and 17 were amended. New claim 25 was added. No claims were canceled. Support for the amendments can be found, for example, on page 25, lines 5-16; on page 27, lines 1-15; on page 38, lines 16-17; on page 49, lines 17-24; and in Figures 4, 5, and 15 of the drawings. This application is believed to be in condition for allowance, and reconsideration is respectfully requested in view of the above amendments and the following comments.

I. 35 U.S.C. § 101

The Examiner has rejected claims 17-18 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

In rejecting the claims, the Examiner asserts that claims 17 and 18 recite code *per se*. Although Applicants believe the claims previously presented fully satisfied the requirements of 35 U.S.C. § 101; in order to expedite prosecution, independent claim 17 has been further amended herein to recite a computer program product comprising "a computer recordable medium having computer usable program code for monitoring execution of instructions." This language further clarifies that the claim is directed to tangible subject matter and clearly satisfies the requirements of 35 U.S.C. § 101.

Therefore, the rejection of claims 17 and 18 under 35 U.S.C. § 101 has been overcome.

II. 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 1-2, 9-10, and 17-18 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> Claims 1-2, 9-10, and 17-18 recites the limitation, 'indicators", where in the claims, this limitation is broadly and it has no adequate function/description for this limitation in the specification, the interpretation for "indicators" is the elements such as the segments of instructions in a program which causes "bottle neck", "cache miss", etc.

Final Office Action dated September 25, 2007, page 4.

Applicants respectfully disagree that the term "indicators" or, more specifically, the term "performance indicators" as is actually used in the claims, is inadequately described in the specification. A "performance indicator" is described, in fact, extensively throughout the specification and is illustrated in the drawings.

For example, Figure 5 and the discussion of Figure 5 on page 26, line 20 to page 27, line 21 explains that the indicators may comprise spare bits within an instruction bundle. Further, Figure 4 and the discussion of Figure 4 on page 25, lines 5 to page 26, line 19 explains that the indicators may be stored in a separate area of storage such as a "performance instrumentation shadow cache." Further, on page 38, lines 16-17 it is described how metadata may be placed into a performance instrumentation shadow cache in association with instructions.

Yet further, it is described throughout the specification that when a performance indicator is associated with an instruction, a signal is sent to a performance monitor unit, which counts events associated with execution of the instruction (see for example, Figures 6A, 6B, and Figure 7 and their description on pages 27-29).

The above-described portions of the specification are examples only of the numerous locations at which performance indicators and their function are described. Applicants respectfully submit that the term "performance indicator" as used in the claims is fully and completely disclosed in the specification, and that the claims fully and completely satisfy the requirements 35 U.S.C § 112, second paragraph.

Therefore the rejection of claims 1-2, 9-10, and 17-18 under 35 U.S.C. § 112, second paragraph, has been overcome.

III. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-2, 9-10, and 17-18 under 35 U.S.C. § 102 as being anticipated by "Intel IA-64 Architecture Software Developer's Manual", Revision 1.1, Vol. 4, No. 245320-002, 7-2001 (hereinafter "Intel"). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Amended claim 1, which is representative of claims 9 and 17 with regards to similarly recited subject matter, recites:

> 1. A method in a data processing system for monitoring execution of instructions, the method comprising:
>
> executing a program;
>
> identifying a routine that is used more than a threshold number of times during execution of the program as a routine of interest;

responsive to identifying the routine of interest during execution of the program, dynamically associating instructions in the identified routine of interest with a set of performance indicators to form a modified routine, wherein the set of performance indicators comprises one of a set of performance indicators comprising one or more bits located in fields within the instructions and a set of performance indicators comprising metadata located in a shadow memory, and wherein the set of performance indicators identify that the instructions are to be monitored; and

responsive to execution of an instruction in the modified routine during continued execution of the program, incrementing a counter, wherein the counter provides a value identifying a number of times that the instruction in the modified routine is executed.

Specifically, Intel fails to teach the features of "identifying a routine that is used more than a threshold number of times during execution of the program as a routine of interest," and "responsive to identifying the routine of interest during execution of the program, dynamically associating instructions in the identified routine of interest with a set of performance indicators to form a modified routine, wherein the set of performance indicators comprises one of a set of performance indicators comprising one or more bits located in fields within the instructions and a set of performance indicators comprising metadata located in a shadow memory, and wherein the set of performance indicators identify that the instructions are to be monitored." Intel does not teach a set of performance indicators as recited in claim 1. The Office Action appears to equate a set of indicators with a set of elements that cause problems such as bottlenecks and so forth. However, claim 1 clearly recites that performance indicators comprise one or more bits located in fields within the instructions or metadata located in a shadow memory. The cited passages of Intel merely recite counting events.

Nowhere does Intel recite a set of performance indicators. Rather, Intel merely teaches that events occur and that those events are counted. In contradistinction, claim 1 recites that once a specific routine is identified, instructions are dynamically associated with the performance indicators, forming a modified routine. Furthermore, the performance indicators are comprised of either one or more bits located in fields within the instructions or metadata located in shadow memory. Nowhere does Intel teach or even hint at identifying a routine and a set of instructions and then dynamically modifying the instructions once they have been identified to include the performance indicators. Furthermore, nowhere does Intel teach or even hint at a set of performance indicators as recited in claim 1. Rather, Intel merely teaches counting an event when an event occurs. Thus, Intel fails to teach the feature of "responsive to identifying the routine of interest during execution of the program, dynamically associating instructions in the identified routine of interest with a set of performance indicators to form a modified routine, wherein the set of performance indicators comprises one of a set of performance indicators comprising one or

more bits located in fields within the instructions and a set of performance indicators comprising metadata located in a shadow memory, and wherein the set of performance indicators identify that the instructions are to be monitored."

Additionally, Intel fails to teach the feature of "identifying a routine that is used more than a threshold number of times during execution of the program as a routine of interest." The Office Action cites to Intel, section 6.1.1.3 as allegedly teaching this feature. However, section 6.1.1.3 of Intel merely teaches running a benchmark program using different threshold values in the various running in order to create a histogram. In contradistinction, claim 1 recites identifying a routine that is used more than a threshold number of times. Thus, Intel teaches running a program multiple times using different threshold values, whereas claim 1 recites identifying a program that is used more than a threshold number of times. Therefore, Intel fails to teach the feature of "identifying a routine that is used more than a threshold number of times during execution of the program as a routine of interest."

Therefore, for at least the reasons set forth above, Applicants submit that Intel fails to anticipate claim 1, as Intel fails to teach each and every feature of claim 1. As claim 1 is representative of claims 9 and 17, the same distinctions between claim 1 and Intel apply to these claims as well. Therefore, Applicants submit that independent claims 1, 9, and 17 are in condition for allowance over the Intel reference. Since claims 2, 10, and 18 depend from claims 1, 9, and 17, the same distinctions between Intel and the claimed invention in claims 1, 9, and 17 apply for these claims. Therefore, Applicants submit that claims 2, 10, and 18 are also in condition for allowance over the cited reference at least by virtue of depending from an allowable claim.

Therefore, the rejection of claims 1-2, 9-10, and 17-18 under 35 U.S.C. § 102 has been overcome.

New claim 25 recites similar subject matter as claim 1, and includes additional subject matter that is neither disclosed nor suggested by Intel. Claim 25, accordingly, also patentably distinguishes over Intel in its present form.

IV. Conclusion

It is respectfully urged that the subject application is patentable over Intel and is now in condition for allowance, and it is respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

/Gerald H. Glanzman/

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